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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM 10021447	FILING DATE 10/30/2001	CLASS 702	SUBCLASS 125	GAU 2857	EXAMINER Bhat
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**APPLICANTS: Chan Siuki; 2863

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH <input checked="" type="checkbox"/>	RESCIND <input type="checkbox"/>	ATTORNEY DOCKET NO X-885 US
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no			
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no			
Verified and Acknowledged Examiners's initials			
TITLE : Methods and circuits for measuring clock skew on programmable logic devices			

U.S. DEPT. OF COMMERCE/PAT. & TM.-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs.Drwg. Print Fig.
		Application Examiner	
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	
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